

General Description

The switch IP implements a 5 Ports solution. One port used as management port with generic 32-bit interface, 4 ports includes integrated MACs. We implementing two 10/100/1000Mbps GMII/MII (eth0,eth1) and two 10/100Mbps MII (eth2, eth3) interfaces.

General purpose 32-bit processor interface for control, no internal CPU

Known limitations:

The following limitations are seen:

The total switching capacity of the switch engine is expected to be less than 1.5 Gbps for any combination. At maximum two of the ports allows to implement Gigabit link in any configuration.

Implementation notes:

The Switch can either operate with forwarding the frames including CRC from/to all ports.

This provides protection throughout the switch and is the recommended mode of operation if no frame manipulation is required. When frame manipulation (VLAN Tag insertion/removal) is required then CRC must be regenerated on all outputs and removed from all inputs. The MACs and Switch support both modes of operation.

Features

- Optional VLAN table for up to 32 VLANs (can be removed for size reduction)
- Optional VLAN manipulation functions (can be removed for size reduction)
- 4 Output Queues per Port with shared memory for all ports; Synthesis Option to increase to 8 Queues per Port
- Shared memory size depending on available on-chip device memory (a minimum of 64Kbyte is suggested); Single Port memory implementation required.
- Priority Classification based on VLAN priorities as well as IPv4 TOS/IPv6 COS with programmable mapping.
- Standard Frame size support (1536) or extended frame sizes up to 1700 bytes.
- MAC (L2) switching with 2048 address table capacity (requires 128Kbit memory)
 - Single Port memory implementation required
 - Hardware learning/aging without software involvement
- MAC per port statistics
- Switch statistics for total frames processed/discarded
- Hardware supports implementation of Rapid Spanning Tree Protocol (RSTP).
 - Requires RSTP software implemented on the external processor: A reference software is provided for porting it to chosen processor environment (porting done by customer).
- Hardware support for use of the switch in AVB environments 802.1as:
 - Enable Peer-to-Peer transparent clock implementation;
 - Integrated MACs to allow timestamp generation;
 - Integrated adjustable timer;
 - Enable forwarding of protocol frames to/from management port;
 - 802.1Qav: Credit based shaper for up to 2 queues per port.
- Hardware enables software on management processor to implement necessary control protocols (802.1at: SRP, 802.1as: PTP) by special forwarding rules for protocol frames to/from management port. Protocol software is not provided.
- Reference software implementing a minimum basic subset of IEEE 1588/802.1 as showing clock synchronization and peer-to-peer transparent clock implementation with the switch hardware.

Functional Description

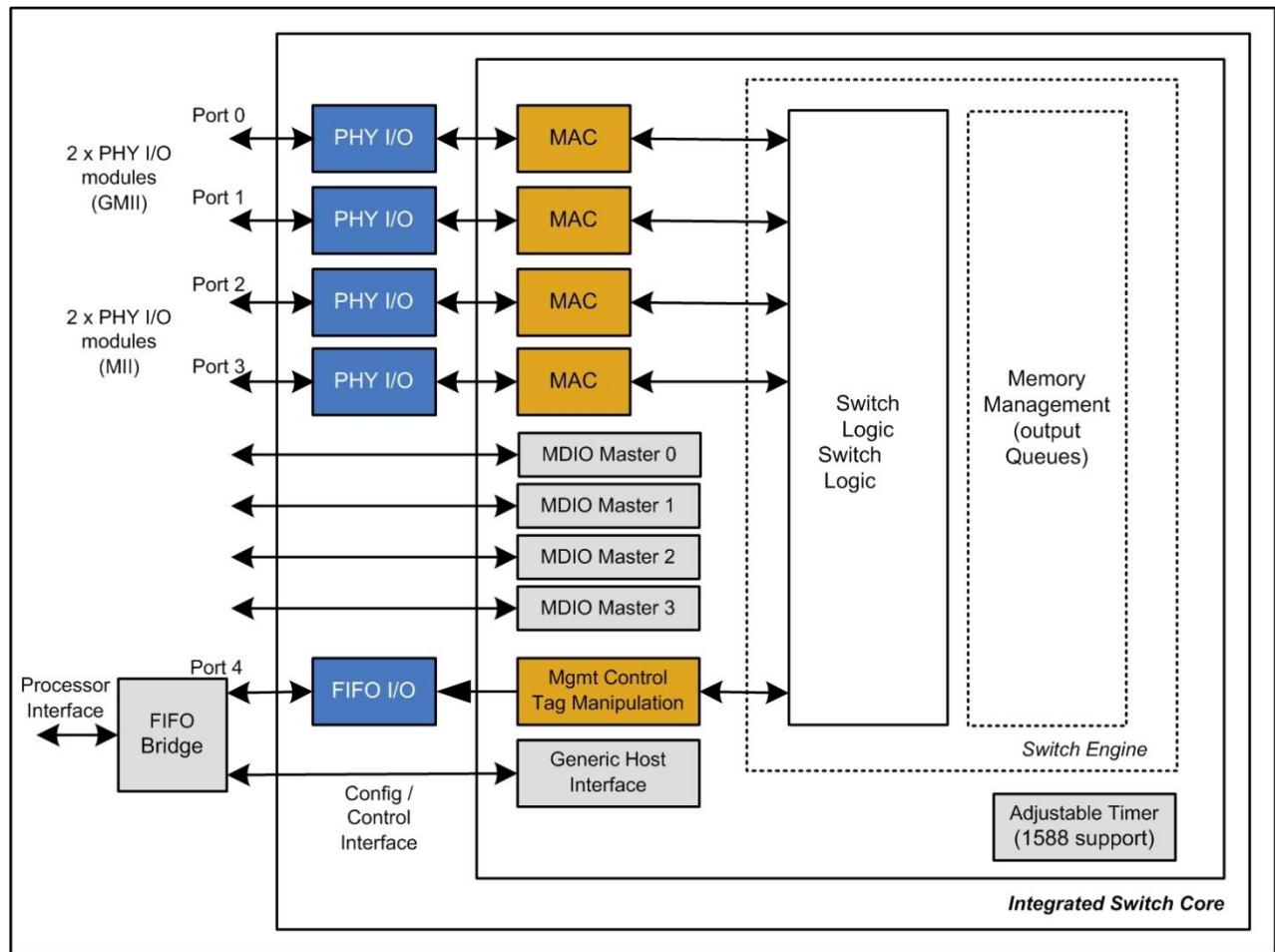
The core includes a 32-bit AMBA AHB system interface.

The core can be handled with our AMBA- IP Manager or standalone.

The core can be delivered only as an encrypted netlist for Altera FPGAs, RTL netlist can be ordered directly from MorethanIP.

LINUX driver available!

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
ARRIA (Altera)	different	Logic Elements: 33129 Block Memory: 592720 bit	100 MHz AHB bus clock