

Provider of IP: GE-Research

Version 1.0

## General Description

The GERA IO-Link Master IP-core with AHB interface is a hardware implementation of the IO-Link master data-link and physical layer with the possibility to maintain multiple IO-Link ports in parallel.

For control and communication with the used IO-Link PHY, a SPI master interface is integrated.

The GERA IO-Link Master IP is developed in close cooperation with TMG in Karlsruhe, leading provider for IO-Link master stack.

## Features

AMBA-IP-core with AHB interface

Implementing...

- IO-Link 1.1 master data link and physical layer,

Supporting...

- IO-Link SIO DI/DO and SDCI COM3/COM2/COM1 mode
- IO-Link Process, Page, SPDU/ISDU and Event/Diagnosis channel
- Automatic WakeUp and ComRequest procedure including detection of transfer rate,

Others...

- Generic number of IO-Link ports and WakeUp pulse length,
- I/O signals match ZMDI ZIOL PHY interface (optimized for use with HC-IOLZ8v2),
- Integrated SPI-IP-core to configure PHY,
- Hardware Abstraction Layer and test software available

## Functional Description

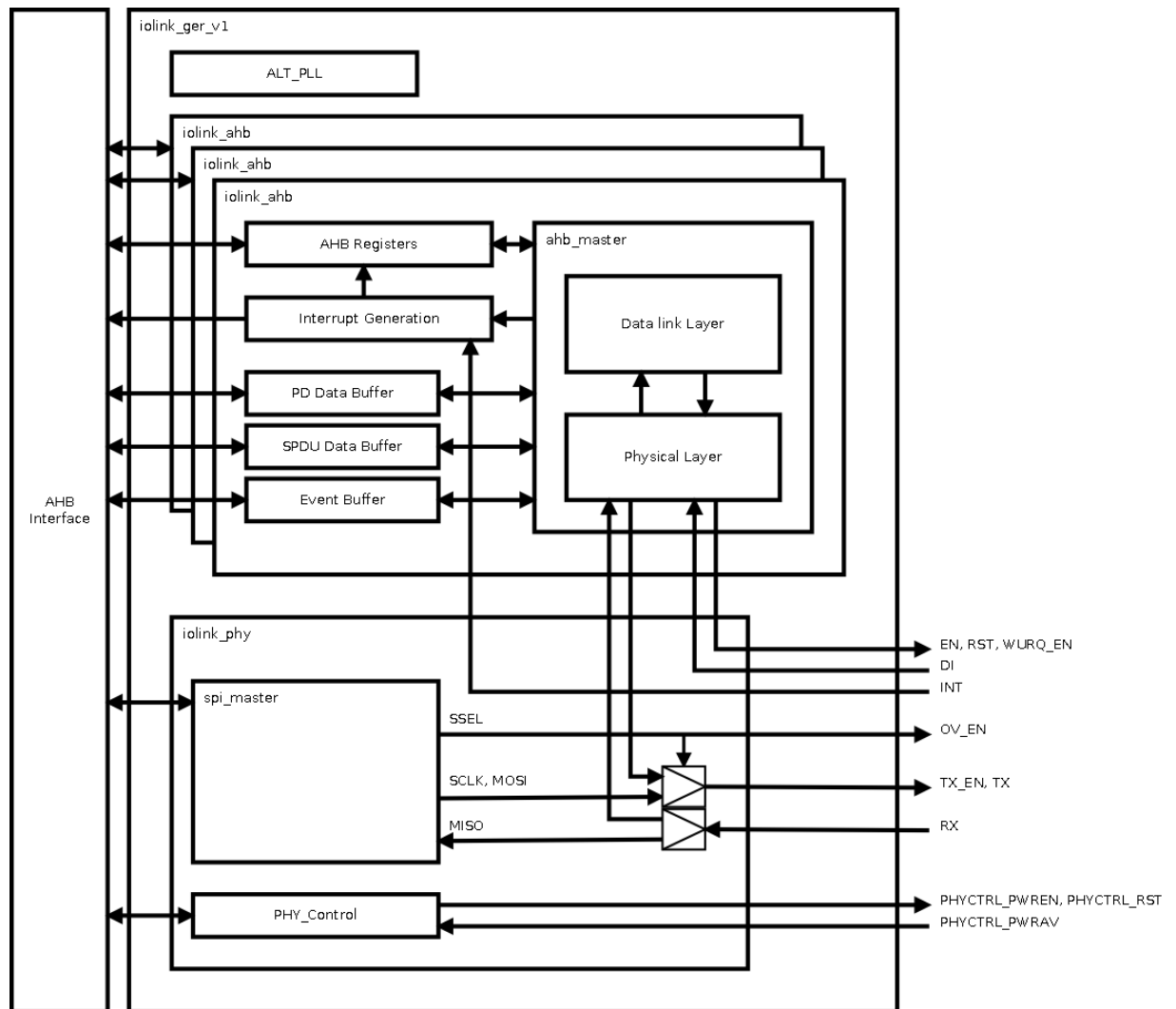
The GERA IO-Link Master IP-core with AHB interface is a hardware implementation of the IO-Link 1.1 master data link and physical layer. The hardware unit for one IO-Link port is internally duplicated up to the number of required ports to facilitate the implementation of a master with multiple ports each connected to one device. As a result a master with any number of IO-Link point-to-point connections to devices in parallel is realizable.

The number of connected phys as well as the number of IO-Link ports to be implemented in hardware can be set via generics. Additionally the duration of a WakeUp pulse can be specified. To control the and communicate with the used IO-Link phy, a SPI master is integrated.

The IP supports all IO-Link physical layer nodes 'Standard I/O' (SIO DI and DO) and 'Single-drop Digital Communication Interface' (SDCI) at transfer rates COM3, COM2 and COM1. On data link layer level the IP supports the common DL modes 'STARTUP', 'PREOPERATE' and 'OPERATE'.

For more information please read the manual.

## Block Diagram



## Device Utilization & Performance

Technology	IO-Link Lines	Utilization (Average out of some different applications)	Performance
ARRIA (2) (Altera)	1	Logic Elements: 2.564 Block Memory: 5.168 bit	100 MHz AHB bus clock
"	4	Logic Elements: 9.478 Block Memory: 20.288bit	"
"	8	Logic Elements: 18828 Block Memory: 40448 bit	"