

### General Description

The GERA SPI Master IP-core is a simple SPI master with AHB interface.

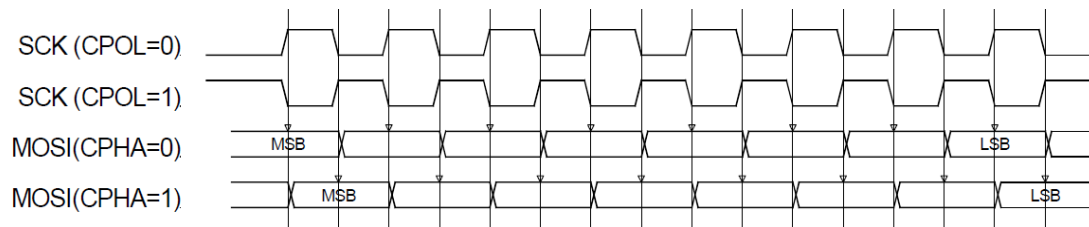
For a minimum of SPI functionality 3 wires (SCKL, MOSI, MISO) are required. To provide flexibility for more use cases the IP-core offers also a slave select (SSEL) and address outputs to communicate with multiple SPI slaves. Address bit width, word bit width and the buffer FIFO depth can be set by generics.

Manual: GERA-SPI-Master Manual V1.0.pdf

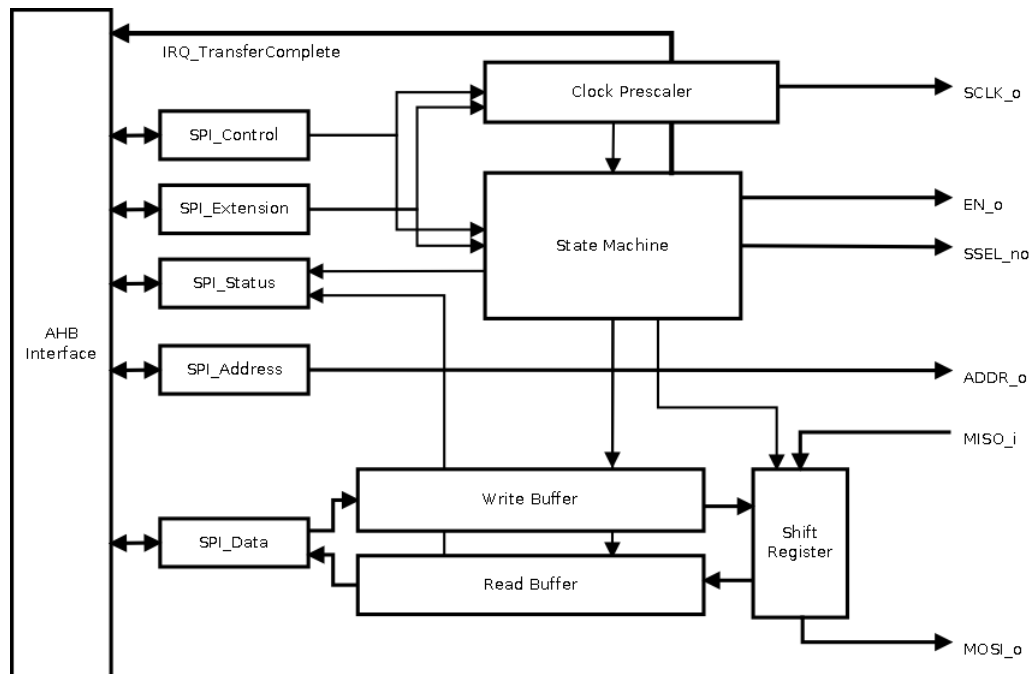
### Features

- AMBA 2.0 AHB interface
- Generics for
  - Bit width of address port
  - Word width of FIFO and shift register
  - FIFO depth of write and read buffer

### Functional Description



### Block Diagram



### Device Utilization & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
ARRIA GX (Altera)	EP1AGX90-C6	Logic Elements: 150 Block Memory: 64 or 128 (8 bit width, FIFO depth of 4 or 8 for Tx and Rx buffer)	100 MHz AHB bus clock