

General Description

Gleichmann Electronics Research provides an AHB Testbench Master which enables to simulate an AIM design and to test its functional behavior. This IP core can initiate an AHB bus communication to read and write from registers of other IP cores.

Manual: GERA-TBM Manual V1.0.pdf

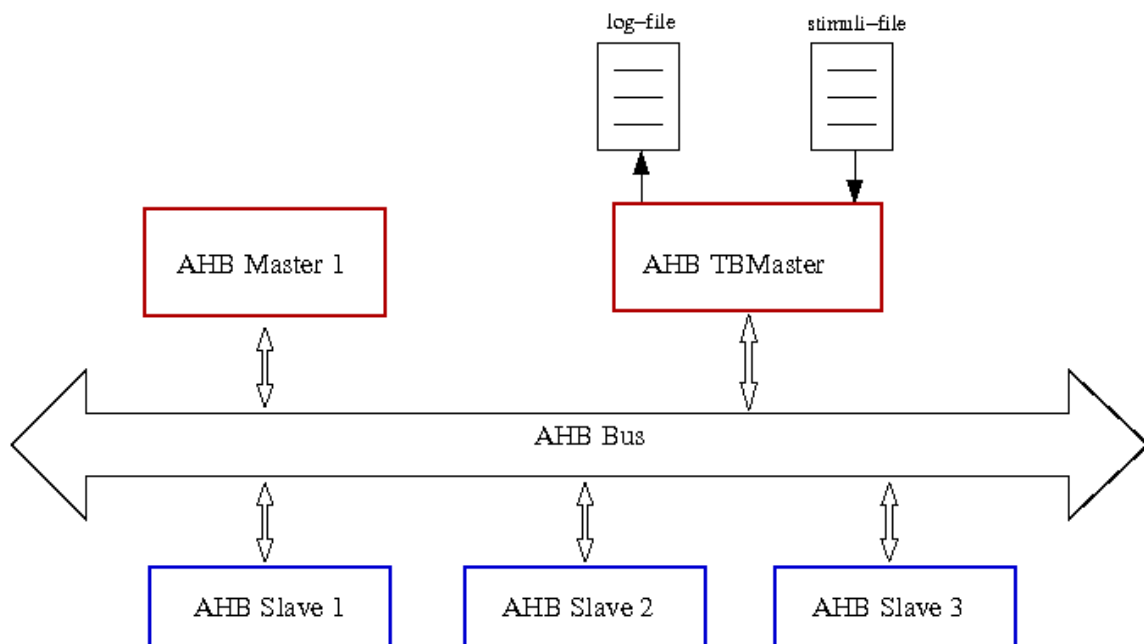
Features

- AMBA 2.0 AHB master and slave interface
- Description of a test driver possible (python script)
- Log the AHB bus communication
- Log interrupt activities
- Integration of external components in the VHDL test bench
- full synthesizable (works like a dummy in hardware)
- multiple AHB TBMaster per design possible
- Mentor ModelSim is supported for simulation
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Functional Description

The AHB TBMaster will be added to the AIM design like any other IP core. After the generation of the design a test driver will be written in python to imitate a communication on the AHB bus. The communication on the AHB bus and the activated interrupts will be logged in a log file by the AHB TBMaster. The HDL simulator Mentor ModelSim is supported to simulate the test system and to watch the signal waveforms. The AHB TBMaster is full synthesizable but it has no effects for the design functionalities in hardware.

Block Diagram



Device Utilization & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
all	all	Logic Elements: 0 Block Memory: 0 bit	