

General Description

I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. It is primarily used in the consumer and telecom market sector and as a board level communications protocol.

We modified this IP and add an AHB bus interface.

Manual: DG_SERCOS_III_A_M_S_SL_V1.1.2.1.3.pdf

Features

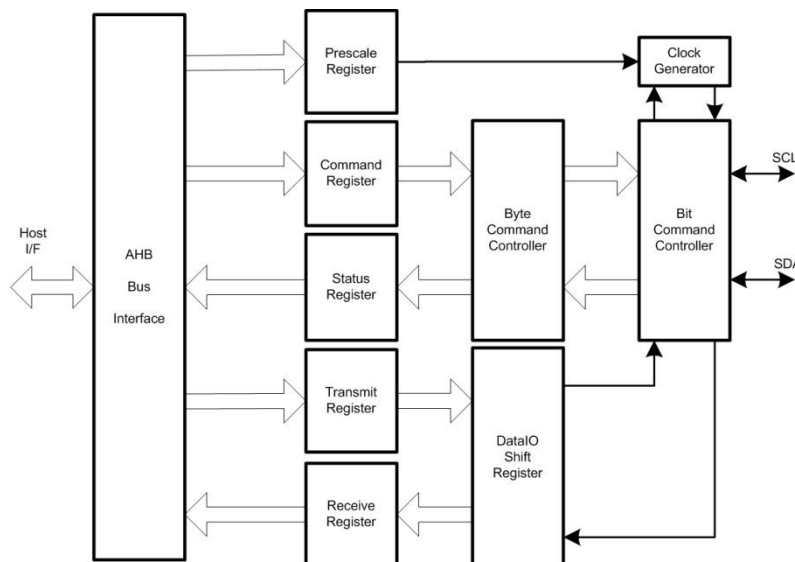
- AMBA 2.0 AHB interface
- Compatible with Philips I2C bus standard
- Multi-Master Operation
- Software programmable timing
- Clock stretching and wait state generation
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancelation
- (Repeated)Start/Stop signal generation/detection
- Bus busy detection
- Supports 7 and 10bit addressing
- Fully static and synchronous design

Functional Description

The I2C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (see START and STOP signals).

Block Diagram



Device Utilisation & Performance

Technology	Device	Utilization (Average out of some different applications)	Performance
Stratix III (Altera)	EP3SL150F780C2	Logic Elements: x Block Memory: 0	100 MHz AHB bus clock
ArriaGX (Altera)	EP1AGX90EF1152C6	Logic Elements: x Block Memory: 0	100 MHz AHB bus clock